AMENDMENTS TO THE SPECIFICATION:

Please amend the title of the invention as follows:

CONTEXT SWITCHING METHOD, ~~DEVICE~~, ~~PROGRAM, RECORDING MEDIUM,~~ CONTEXT SWITCHING UNIT, CONTEXT SWITCHING PROGRAM, STORAGE MEDIUM, AND CENTRAL PROCESSING UNIT

On page 1 after the title, please insert the following:

CROSS - REFERENCE TO RELATED APPLICATIONS

The present Application is based on International Application No. PCT/JP2003/015838, filed on December 11, 2003, which in turn corresponds to JP 2003-3038 filed on September 1, 2003, and priority is hereby claimed under 35 USC §119 based on these applications. Each of these applications are hereby incorporated by reference in their entirety into the present application.

Please amend the third paragraph on page 10, line 32 as follows:

Then, the software, such as an OS, uses a load instruction to restore a new context to be executed. After the current context is saved, the software, such as an OS, issues a load instruction. When the load instruction is issued, the memory access unit 5 calculates a data read address and accesses the data cache 6 (S111). If a data cache error occurs (S113), the data cache 6 reads a cache line from the memory 20 (S115). If no data cache error occurs (S113), the processing proceeds to step S117. When data is returned from the data cache 6 (S117), the memory access unit 5 writes the data back into the register file 1. The load instruction is processed as many times as the number of registers to be restored. When the contents of all the registers are not read, the processing is repeated back

Please amend the fourth paragraph on page 11, line 22 as follows:

The context cache 8 uses a SRAM, a FF, and other elements, and can process an access, a read, a write, and others at a high processing speed. The context cache 8 is connected to the register file 1 via the context switching bus 12, and is used to cache a context. The thread control ~~unit 8~~ unit 9 is a unit for controlling the context cache 8 and is connected in parallel with the ALU 4 and the memory access unit 5. A thread generally means a processing unit or the smallest unit into which a process or a task is divided when the OS performs parallel processing of processes or tasks. Some processes or tasks may not be divided, and one process or one task may become one thread. When a context switch occurs, the context (a general-purpose register, a floating-point register, a program counter, a status register, and others) of the current thread must be saved, and the context of a new thread to be executed must be restored. When the

Please amend the second paragraph on page 15, lines 19 and 20 as follows:

The register file 1 has a normal read port, a normal write port, and also special ports for context switching, which are a context-switching read port 17 and a context-switching write port 18, and a storage unit for holding a context is connected to these ports. In the shown embodiment, the register file 1 has a register read port 15, a register write port 16, the context-switching read port 17, and the context-switching write port 18. The register read port 15 is a port for reading a register from the register file 1 to a unit in the CPU; the register write port 16 is a port for writing a register from a unit in the CPU to the register file 1; the context-switching read port 17 is a port for reading a register from the register file 1 to the context ~~file 8~~ cache 8 ; and the context-switching write port 18 is a port for writing a register from the context ~~file 8~~ cache 8 to the register file 1.